Ni DOPING EFFECTS ON INDUCTANCE AND NEGATIVE CAPACITANCE IN MPS DEVICES

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This study presents a comprehensive investigation of the negative capacitance behavior in Metal–Semiconductor (Au/n-Si MS) and Metal–Polymer–Semiconductor (MPS) structures (Au/Pure PVP/n-Si-MPS1 and Ni-doped PVP/n-Si-MPS2 and MPS3 SDs), by correlating capacitance–voltage (C–V) characteristics with the voltage-dependent effective inductance L(V) in the bias interval of 2.0–3.6 V at 300 K. In this negative capacitance regime, the delayed response of interface and bulk traps produces a phase-shifted current, which manifests as a positive imaginary component in the impedance and can be interpreted as an effective inductive behavior. The L(V) curves extracted from the negative C–V regions exhibit a highly linear dependence on applied bias, with regression coefficients R^2 exceeding 0.985, confirming a uniform and single-mechanism trap response over the studied voltage range. The slopes dL/dV obtained from linear fits are approximately 6×10^{-6} H/V for MPS1, 5×10^{-6} H/V for MS, and 2×10^{-6} H/V for MPS2 and MPS3, where steeper slopes directly correspond to higher trap densities and longer effective charge relaxation times, while shallower slopes indicate fewer active traps or faster trap emission. The nearly zero second derivative d^2L/dV^2 demonstrates that the trap response is highly linear without noticeable nonlinear activation or saturation effects in this voltage interval. Complementary negative C–V measurements further validate the inductive interpretation, as the onset and evolution of negative capacitance are directly linked to the trap-mediated dynamic processes within the polymer interlayer and at the semiconductor interface. This combined slope–capacitance analysis provides a powerful framework for probing interfacial and bulk trap dynamics in MS and MPS structures, revealing that MPS1 exhibits the most pronounced negative capacitance and strongest trap activity.

Keywords: Negative capacitance, Metal–Polymer–Semiconductor (MPS) structures, Voltage-dependent inductance, Trap dynamics, Capacitance–voltage (C–V) characteristics, Interface states.
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INTRODUCTION

The study of metal–polymer–semiconductor (MPS) structures has emerged as a vibrant research area in electronic materials science because these hybrid interfaces offer a unique platform where polymeric dielectrics can actively modulate the electronic behavior of traditional metal–semiconductor junctions. The introduction of a thin polymer interlayer modifies interface states, alters surface potential distribution, and enhances device tunability by introducing additional charge storage and trapping mechanisms. Among the diverse polymer candidates for such applications, polyvinylpyrrolidone (PVP) has attracted considerable attention due to its high chemical stability, excellent film-forming properties, and ability to be doped with transition metals, which can create controllable trap levels and induce interfacial dipole moments [1-7]. When a gold (Au) top electrode is deposited on metal-doped PVA films over n-type silicon (n-Si), the resulting MPS structure combines the rectifying nature of the Schottky junction with the dynamic charge storage properties of the polymeric layer. This hybrid configuration offers opportunities for designing high-performance electronic devices such as sensors, memories, and negative capacitance-based circuits. But, there are not enough information structures of Ni doped PVP as interfacial layer on MPS in literature [7-12].

In analog integrated circuits and other electronic systems, inductors are used, which creates a number of problems [4,13,14]. In recent years, scientists have focused their attention on creating analogs of inductance, forming circuit elements with inductive impedance using new technologies and circuit techniques. In this regard, structures with negative capacitance equivalent to inductance attract much attention [13-26].

One of the most fascinating phenomena observed in polymer-modified semiconductor junctions is the occurrence of negative capacitance (NC) under certain biasing and frequency conditions. Negative capacitance is an anomalous regime in which the measured capacitance of the device becomes negative, implying that the current leads the applied voltage rather than lagging behind as in conventional capacitive behavior [3,4]. Physically, this phenomenon is generally attributed to delayed trap response, interface state dynamics, and carrier capture–emission processes within the polymer interlayer and at the semiconductor interface. In such scenarios, the AC signal drives carriers into traps that release them out of phase with the applied voltage, effectively producing a current response characteristic of an inductive element [3,4,13-26]. This behavior is of both fundamental and practical interest because negative capacitance has been linked to performance enhancement in electronic devices, reduced subthreshold slope in transistors, and novel oscillatory or memory effects.

In the present study, we systematically investigate the electrical properties of Au/Ni-doped PVP/n-Si MPS structures at room temperature (300 K) under a 500 kHz AC test signal, focusing specifically on the negative capacitance regime and its equivalent inductive characterization. It is known that such a phenomenon is observed in structures with inertial-

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relaxation conductivity, when the reactive component of the total conductivity exceeds the Maxwellian displacement current. The devices were biased over a voltage range that captures the transition from normal capacitive behavior to negative capacitance, and detailed capacitance–voltage (C–V) measurements were performed to map the response. Our C–V characteristics reveal that beyond approximately 2 V, the capacitance drops below zero, signifying the onset of negative capacitance behavior. This transition indicates that the dynamic trapping and de-trapping processes within the Ni-doped PVP layer and at the PVP/n-Si interface have reached a regime where the out-of-phase current dominates the response. Such behavior is particularly enhanced in our samples due to the Ni doping, which introduces additional localized states that can act as fast and slow traps, contributing to the observed phase shift. These studies are of interest because they create prospects for the creation of inductance analogs, methods for manufacturing multifunctional devices based on Schottky diodes in a single technological process. In addition, based on the results of the study, the causes of the appearance of inductive impedance can be identified.

EXPERIMENTAL DETAILS

In this study, Au/n-Si Schottky diodes (SDs) were prepared both with and without polyvinylpyrrolidone (PVP) interlayers, including undoped PVP as well as 3% and 5% Ni-doped PVP films, using identical phosphorus-doped n-type silicon wafers. The wafers, oriented along the (100) plane, were about 350 μm thick and had a resistivity of 1–10 Ω·cm. Each wafer was divided into two pieces and cleaned to eliminate the native oxide layer and any surface impurities. The cleaning procedure involved immersing the wafers in an ammonium peroxide solution for 1 minute, then dipping them in an acidic mixture of H_2SO_4:H_2O_2:H_2O (3:1:1) for 3 minutes. Afterward, the wafers were rinsed with high-purity deionized water (18 MΩ·cm) for 10 minutes and dried with nitrogen gas. A 150 nm layer of 99.99% pure gold (Au) was then thermally evaporated onto the back side of each wafer under a high vacuum of 10^{-6} Torr to form the ohmic contact. The contacts were stabilized by annealing at 550 °C for 5 minutes in a nitrogen atmosphere to ensure low resistance. On the front side of the first wafer section, circular Au dots with an active area of 7.85×10^{-3} cm² were deposited to create reference Au/n-Si Schottky diodes. On the second wafer section, 3% and 5% Ni-doped PVP solutions were applied to the front surface by electrospinning, forming uniform polymer layers. Au dots of the same size were then deposited on these layers to produce Au/(3% or 5% Ni-PVP)/n-Si metal–polymer–semiconductor (MPS) diodes.

Electrical measurements were performed by connecting the front and back electrodes with silver-coated copper wires. Both the rectifying front contacts and the ohmic back contacts were made using a high-vacuum thermal evaporation system equipped with a stainless-steel sample holder. The thickness of the Au layers was continuously monitored using a precision metal thickness gauge during the entire process.

RESULTS AND DISCUSSIONS

The occurrence of negative capacitance, inductive impedance, known from scientific literature, is explained by various reasons, which are caused by the choice of the structure under study, the conditions of the experiment, and the influence of external influences [3,4,13-17]. Fundamentally, negative capacitance arises when the rate of change of charge with respect to voltage is inverted due to delayed responses of interface or bulk polarization mechanisms. In the case of our samples (Au/n-Si, Au/Pure PVP/n-Si and Ni-doped PVP/n-Si SDs), the interfacial traps and localized defect states act as temporary reservoirs for charge carriers. Under an AC signal, these traps capture and release charges out of phase with the applied voltage, leading to a phase shift in the current that manifests as an effective negative capacitance. For all structures it is characteristic that there is such a frequency value at which the reactive component of the full admittance exceeds the Maxwellian displacement current [3,4,13-26]. In this case, the inductive properties are determined by a series circuit with elements R and L. In such structures, the inductance value can be calculated from the negative capacitance values [3,4,27]. The appearance of negative capacitance reveals the transition from capacitive-type impedance to inductive-type impedance. The parallel circuit of elements R and C is replaced by a series circuit of elements R and L [13-18,27]. In general, the inductance is defined by our as

$$L = \frac{R^2(-C)}{1+\omega^2 R^2 C^2} \quad (1)$$

First of all, we show negative capacitance part in Fig 1. In the low-bias region of 2.0–2.5 V, the inductance increases approximately linearly with applied voltage, reflecting the regime where the negative capacitance scales proportionally with bias as showing in Fig 2.

This linearity indicates that the trap states are actively participating in polarization dynamics, with their response strongly dependent on the applied electric field. Among our samples, the undoped MPS1 structure exhibits the steepest increase in inductance with voltage, revealing that it possesses the highest density of active traps and, therefore, the strongest negative capacitance effect. The pure MS sample follows with a slightly lower slope, indicative of fewer interfacial states, while the Ni-doped MPS2 and MPS3 samples exhibit markedly reduced slopes. This reduction in slope directly reflects the role of Ni doping in passivating trap states at the polymer/semiconductor interface and suppressing delayed polarization, thereby diminishing the negative capacitance contribution to the equivalent inductance.

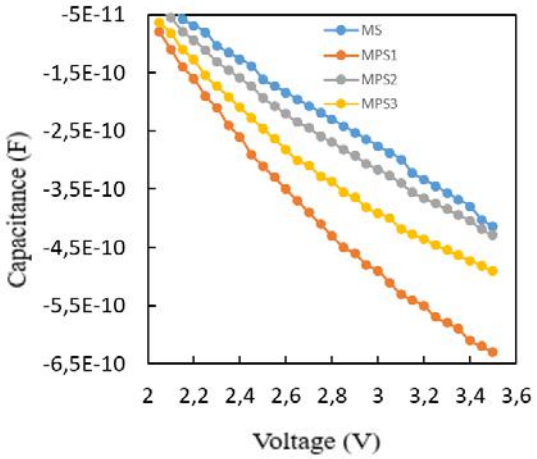

Fig 1. Negative capacitance for MS and MPS1, MPS2, MPS3 structures.

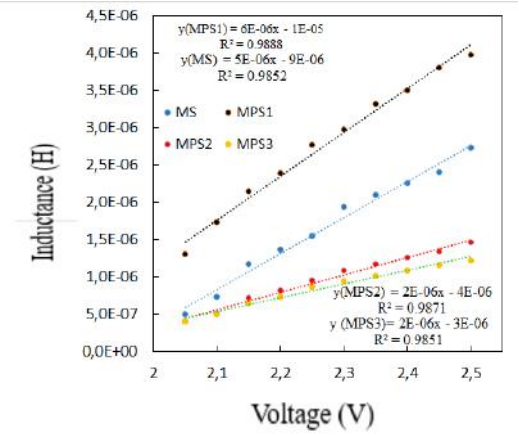

Fig 2. Linear part of inductance for MS and MPS1, MPS2, MPS3 structures.

As the bias extends toward 3.4 V, the L–V characteristics become nonlinear, with inductance initially rising, reaching a peak, and then showing signs of saturation or mild decline as representing Fig 3. This behavior corresponds to trap saturation [3,4]. At low to moderate biases, the increasing electric field energizes a growing population of traps to participate in delayed charge dynamics, but as the majority of traps become filled, additional bias does not significantly enhance negative capacitance, leading to the observed saturation of inductance. The sample hierarchy remains consistent across this regime, with MPS1 displaying the highest inductance and MPS3 the lowest. This pattern reflects a clear and systematic influence of Ni doping: as the concentration of Ni increases, the density of effective trap states decreases, interfacial polarization is damped, and the negative capacitance effect is gradually suppressed.

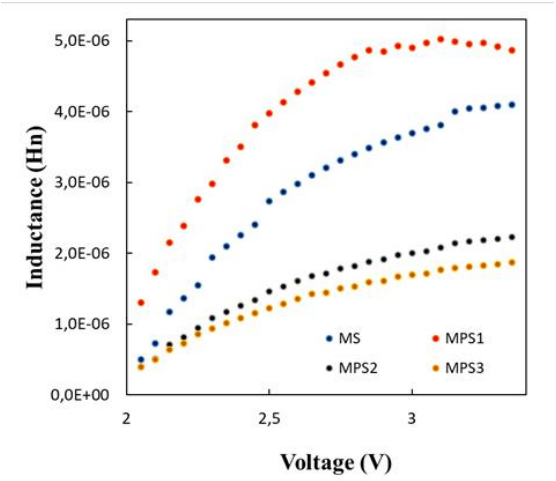

Fig 3. Inductance for MP and MPS1, MPS2, MPS3 structures

Nickel incorporation interacts with the polymer and the underlying semiconductor in a manner that passivates defect sites and reduces charge trapping. This structural modification has a dual effect: it mitigates the delayed polarization responsible for negative capacitance and simultaneously stabilizes the dielectric response under varying bias conditions. Consequently, as the Ni content increases from MPS1 (undoped) to MPS3 (highly doped), the magnitude of negative capacitance diminishes, the peak inductance decreases, and the slope of the L–V curve flattens.

CONCLUSION

Ni doping exerts a profound influence on the electrical response of MPS devices, systematically suppressing negative capacitance and stabilizing interfacial dynamics. In the undoped MPS1 sample, the high density of active trap states produces the largest negative capacitance and the steepest dL/dV slope, reflecting strong interfacial polarization and bias sensitivity. As Ni is introduced in MPS2, partial trap passivation occurs, reducing both the negative capacitance magnitude and slope, leading to smoother and more controlled L-V behavior. At high Ni doping levels in MPS3, most interfacial traps are neutralized, resulting in minimal negative capacitance, the lowest slope response, and a transition toward conventional capacitive behavior with weak bias dependence. This progressive evolution from trap-driven instability to stable capacitive operation demonstrates that Ni doping is an effective strategy for tailoring interfacial charge dynamics, suppressing delayed polarization effects, and achieving reliable device performance. The slope analysis (dL/dV) further provides a quantitative indicator of interfacial activity, confirming that higher slopes correspond to energetic, trap-rich systems, while lower slopes mark passivated, stable interfaces. Overall, Ni doping not only mitigates negative capacitance but also enables a controlled transition from unstable to robust electrical behavior, offering valuable insights for the design of advanced electronic and energy storage devices.

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